

Atty Docket No. 012172-004530US

PTO FAX NO.: 1-703-308-6306

ATTENTION: Examiner Viet Vu  
Group Art Unit 2758

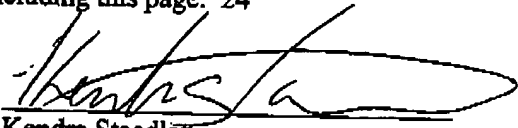
**OFFICIAL COMMUNICATION**  
**FOR THE PERSONAL ATTENTION OF**  
**EXAMINER VIET VU**

**CERTIFICATION OF FACSIMILE TRANSMISSION**

I hereby certify that the following: After Final Amendment in re Application of Howard G. Sachs, Application No. 09/057,861, filed April 9, 1998, for INSTRUCTION CACHE ASSOCIATIVE CROSSBAR SWITCH is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

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Dated: January 22, 2001

  
Kendra Staedler

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I hereby certify that this correspondence is being sent by facsimile transmission to:

Examiner Viet Vu  
at Fax No.: 1-703-308-6306

On January 22, 2001  
TOWNSEND and TOWNSEND and CREW LLP

By: [Signature]

Attorney Docket No.: 12172-004530US

PATENT



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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Howard G. Sachs

Application No.: 09/057,861

Filed: April 9, 1998

For: INSTRUCTION CACHE  
ASSOCIATIVE CROSSBAR SWITCH

Box AF

Assistant Commissioner for Patents  
Washington, D.C. 20231

Examiner: V. Vu

Art Unit: 2758

SUPPLEMENTAL AMENDMENT AND  
REQUEST FOR INTERFERENCE  
WITH U.S. PATENT NO. 5,922,065  
UNDER 37 C.F.R. §1.607

Sir:

In response to the Office action dated October 24, 2000 and to our recent telephone interview, please enter the following remarks.

139. (Amended) A processor comprising:  
a register file having a plurality of registers;  
an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;  
a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;  
and further wherein the instructions are encoded in frames, each frame including a plurality of instructions and routing data grouped together in an N-bit field, the instructions being located in instruction positions of the N-bit field, the routing data specifying a routing of the instructions in the instruction positions to the execution unit types ;  
wherein the routing data is not primarily determined by hardware.